What is claimed is:

1. A process comprising:

providing a recess in a substrate, wherein the recess comprises three monolithic crystallographic surfaces;

first processing the recess under conditions to cause the recess to form a localized epitaxial semiconductor film comprising more than three monolithic crystallographic surfaces; and

forming an electrode in the recess.

2. The process according to claim 1, further including:

second processing the recess under conditions to anneal at least a portion of the more than three monolithic crystallographic surfaces.

3. The process according to claim 1, further including:

second processing the recess in a hydrogen-type atmosphere to anneal at least a portion of the more than three monolithic crystallographic surfaces.

4. The process according to claim 1, further including:

forming a dielectric layer over the epitaxial semiconductor film; and

filling at least a portion of the recess with an electrical conductor.

5. The process according to claim 1, further including:

forming a dielectric layer over the epitaxial semiconductor film, wherein the dielectric layer is selected from a refractory metal oxide, a thermal oxide, a silicon oxide, a silicon oxynitride, a silicon nitride, a carbon-doped oxide, and combinations thereof; and

filling at least a portion of the recess with an electrical conductor.

6. The process according to claim 1, wherein forming an electrode further includes:
forming a dielectric layer over the epitaxial semiconductor film;
filling at least a portion of the recess with doped polysilicon; and
forming a dielectric layer over the doped polysilicon.

7. The process according to claim 1, wherein first processing includes:
providing a reaction chamber;
locating the substrate in the reaction chamber; and
metering a hydrogen-containing composition into the reaction chamber.

8. The process according to claim 1, wherein first processing includes:
providing a reaction chamber;
locating the substrate in the reaction chamber;
metering a hydrogen-containing composition into the reaction chamber; and
heating the reaction chamber to a temperature in a range from about 900° C to about 1,200° C.

9. The process according to claim 1, wherein first processing includes:
providing a reaction chamber;
locating the substrate in the reaction chamber;
metering a hydrogen-containing composition into the reaction chamber at a rate from about 50 sccm to about 10 slm; and
heating the reaction chamber to a temperature in a range from about 900° C to about 1,200° C, from about 10 seconds to about 120 seconds, and at a pressure from about 1 milliTorr to about 1 atmosphere.

10. A process of making a vertical transistor in a substrate, comprising:
forming a shallow trench isolation (STI) structure in a substrate;
etching a recess in the substrate, wherein the recess exposes the substrate with a substrate bottom and two substrate sidewalls, and wherein the recess exposes the STI

structure with an STI sidewall; and

forming an epitaxial semiconductor film in the recess, wherein the epitaxial semiconductor film is disposed over the substrate bottom and two substrate sidewalls.

11. The process according to claim 10, wherein forming an epitaxial film in the recess includes:

first processing the recess in a rapid thermal processing chamber, by heating in a temperature range from about 900° C to about 1,200° C, for a processing time from about 10 seconds to about two minutes, in a hydrogen-type atmosphere, at a pressure from about 1 milliTorr to about one atmosphere, and at a flow rate from about 50 standard cubic centimeters per minute to about 10 standard liters per minute.

12. The process according to claim 10, wherein the epitaxial semiconductor film is disposed over the substrate bottom and two substrate sidewalls to a first amount, and wherein a polysilicon film is disposed over at least a portion of the STI sidewall to a second amount, wherein the first amount is more than the second amount.

13. The process according to claim 10, further including:

second processing the recess in a hydrogen-type atmosphere to anneal at least a portion of the epitaxial semiconductor film that exposes the substrate.

14. The process according to claim 10, further including:

second processing the recess in a hydrogen-inert gas atmosphere to anneal at least a portion of the epitaxial semiconductor film that exposes the substrate, wherein the ratio of hydrogen to inert gas varies from about 2% hydrogen to about 100% hydrogen.

15. The process according to claim 10, further including:

second processing the recess comprising a deuterium-inert gas atmosphere to anneal at least a portion of the epitaxial semiconductor film that exposes the substrate,

wherein the ratio of deuterium to inert gas varies from about 2% deuterium to about 100% deuterium.

16. The process according to claim 10, further including:

forming a dielectric layer over the epitaxial film, wherein the dielectric layer is selected from a refractory metal oxide, a thermal oxide, a silicon oxide, a silicon oxynitride, a silicon nitride, a carbon-doped oxide, and combinations thereof; and

filling at least a portion of the recess with an electrical conductor.

17. A process of forming a vertical transistor comprising:

etching a recess in an upper surface of a semiconductor substrate, wherein the recess is bounded by an upper surface and wherein the recess comprises a bottom and two sidewalls; and

first processing the recess under conditions to cause the recess to form an epitaxial semiconductor film, wherein epitaxial semiconductor film comprises a minor thickness at a region that is closer to the upper surface than to the bottom and a major thickness that is closer to the bottom than to the upper surface.

18. The process according to claim 17, further including:

second processing the recess with a hydrogen-type gas under conditions to anneal at least a portion of the epitaxial semiconductor film.

19. The process according to claim 17, further including:

forming a dielectric layer over the epitaxial semiconductor film; and

filling at least a portion of the recess with an electrical conductor.

20. The process according to claim 17, further including:

forming a shallow trench isolation (STI) structure in the substrate; and

forming the recess immediately adjacent to the STI structure.

21. The process according to claim 17, wherein the semiconductor substrate includes a <100> monocrystalline material, and wherein first processing includes:

providing a reaction chamber;

locating the semiconductor substrate in the reaction chamber;

metering a hydrogen-containing substance into the reaction chamber at a rate from about 50 sccm to about 10 slm; and

heating the reaction chamber to a temperature in a range from about 900° C to about 1,200° C, from about 10 seconds to about 120 seconds, and at a pressure from about 1 milliTorr to about 1 atmosphere.

22. A process of forming a vertical transistor comprising:

forming a shallow trench isolation (STI) structure in an upper surface of a monocrystalline semiconductor substrate;

dry etching a recess to form a recess bottom that is immediately adjacent to the STI; and

treating the recess in a hydrogen-type atmosphere under conditions to cause the monocrystalline semiconductor substrate to form an epitaxial semiconductor layer.

23. The process according to claim 22, wherein the conditions form the epitaxial layer with a minor thickness at a region that is closer to the upper surface than to the bottom and a major thickness that is closer to the bottom than to the upper surface.

24. The process according to claim 22, wherein treating the recess in hydrogen-type atmosphere is carried out under conditions to form an epitaxial semiconductor layer with a with a segmented-surface profile.

25. The process according to claim 22, further including:

forming a dielectric layer over the epitaxial semiconductor layer; and

filling at least a portion of the recess with an electrical conductor.

26. A process comprising:

providing a substrate including an upper surface;

providing a recess in the substrate, wherein the recess includes three monolithic crystallographic surfaces;

first processing the recess under conditions to cause the recess to form a localized epitaxial semiconductor film including more than three monolithic crystallographic surfaces;

doping a portion of the recess, selected from bottom doping, angled implantation, and combinations thereof; and

forming an electrode in the recess.

27. The process according to claim 26, further including:

second processing the recess under conditions to anneal at least a portion of the more than three monolithic crystallographic surfaces.

28. The process according to claim 26, further including:

forming a source and a drain at the upper surface, and wherein doping a portion of the recess is carried out where the source and drain are selected from an N-type dopant and a P-type dopant, and the bottom doping is selected from P- -, P-, P, P+, P++, N- -, N-, N, N+, and N++.

29. The process according to claim 26, further including:

forming a source and a drain at the upper surface, and wherein doping a portion of the recess is carried out where the source and drain are selected from an N-type dopant and a P-type dopant, and the angled implantation is selected from P- -, P-, P, P+, P++, N- -, N-, N, N+, and N++.

30. The process according to claim 26, wherein forming an electrode further includes:

forming a dielectric layer over the epitaxial semiconductor film, wherein the

dielectric layer is selected from a refractory metal oxide, a thermal oxide, a silicon oxide, a silicon oxynitride, a silicon nitride, a carbon-doped oxide, and combinations thereof; and

filling at least a portion of the recess with an electrical conductor.

31. A process of making a computer system, comprising:

forming a processor;

forming a memory system coupled to the processor;

forming an input/output circuit coupled to the processor and the memory system; and

forming a vertical transistor in at least one of the processor, the memory system, and the input/output circuit, forming a vertical transistor including:

providing a recess in a substrate, wherein the recess comprises three monolithic crystallographic surfaces; and

first processing the recess under conditions to cause the recess to form an epitaxial semiconductor film comprising more than three monolithic crystallographic surfaces.

32. The process according to claim 31, further including:

second processing the recess under conditions to anneal at least a portion of the more than three monolithic crystallographic surfaces.

33. A vertical transistor, comprising:

a semiconductor substrate comprising an upper surface;

a recess disposed in the upper surface, wherein the recess contains a localized epitaxial semiconductor film comprising more than three monolithic surfaces;

a gate dielectric layer disposed over the localized epitaxial semiconductor film; and

an electrode disposed in the recess over the gate dielectric layer.

34. The vertical transistor according to claim 33, wherein the electrode has an electrode upper surface that is below the substrate upper surface.

35. The vertical transistor according to claim 33, further including:

a silicon-deuterium transition layer, or a silicon-hydrogen transition layer, or a silicon-hydrogen-deuterium transition layer disposed between the more than three monolithic surfaces and the gate dielectric layer.

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36. The vertical transistor according to claim 33, wherein the gate dielectric layer is selected from a refractory metal oxide, a thermal oxide, a silicon oxide, a silicon oxynitride, a silicon nitride, a carbon-doped oxide, and combinations thereof.

37. The vertical transistor according to claim 33, wherein the electrode is doped polysilicon.

38. The vertical transistor according to claim 33, wherein substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess.

39. The vertical transistor according to claim 33, wherein substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess; and

wherein the source and drain are bounded in a first dimension by a structure having a minimum photolithographic feature.

40. The vertical transistor according to claim 33, wherein substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess;

wherein the source and drain are bounded in a first dimension by a first STI structure having a first minimum photolithographic feature; and

wherein the source or the drain is bounded in a second dimension by a second STI structure having a second minimum feature dimension that is substantially equal to the first minimum feature dimension.

41. The vertical transistor according to claim 33, wherein substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess;

wherein the source and drain are bounded by a first STI structure;

wherein the source or the drain is bounded by a second STI structure;

wherein the recess is disposed in the substrate to a first depth; and

wherein the STI structures are disposed in the substrate to a second depth, and wherein the second depth is greater than the first depth.

42. The vertical transistor according to claim 33, wherein substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess;

wherein the N+ doped source and the N+ doped drain are bounded in a first dimension by a first STI structure;

wherein the N+ doped source and the N+ doped drain are bounded in a second dimension by a second STI structure; and

wherein the STI structures are each disposed within a recess including a curvilinear epitaxial film.

43. An electrical device comprising:

a substrate comprising an upper surface;

an active area disposed in the substrate comprising a source and a drain;

a recess disposed between the source and the drain, wherein the recess comprises a substantially curvilinear bottom profile of epitaxial semiconductive material;

a gate dielectric layer disposed over the epitaxial semiconductive material; and

an electrode disposed over the gate dielectric layer.

44. The electrical device according to claim 43, wherein the electrode has an electrode upper surface that is below the substrate upper surface.

45. The electrical device according to claim 43, further including:

a silicon-deuterium transition layer, or a silicon-hydrogen transition layer, or a silicon-hydrogen-deuterium transition layer disposed between the substantially curvilinear bottom profile of epitaxial semiconductive material and the gate dielectric layer.

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46. The electrical device according to claim 43, wherein the gate dielectric layer is selected from a refractory metal oxide, a thermal oxide, a silicon oxide, a silicon oxynitride, a silicon nitride, a carbon-doped oxide, and combinations thereof.

47. The electrical device according to claim 43, wherein the electrode is doped polysilicon.

48. The electrical device according to claim 43, wherein substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess; and

wherein the source and drain are bounded in a first dimension by a first shallow trench isolation structure comprising a minimum photolithographic feature.

49. The electrical device according to claim 43, wherein the substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess;

wherein the source and drain are bounded in a first dimension by a first shallow trench isolation structure comprising a minimum photolithographic feature; and

wherein the source and the drain are bounded in a second dimension by a second shallow trench isolation structure including the minimum photolithographic feature.

50. An electrical device comprising:

a monocrystalline semiconductor substrate including an upper surface;

an active area disposed in the monocrystalline semiconductor substrate including a source and a drain;

a recess disposed between the source and the drain;

wherein the recess includes a substantially curvilinear bottom profile comprising epitaxial semiconductive material;

a gate dielectric layer disposed over the epitaxial semiconductive material in the recess;

an electrode disposed in the recess; and

a first shallow trench isolation (STI) structure disposed in the monocrystalline semiconductor substrate, wherein the recess exposes at least a portion thereof.

51. The electrical device according to claim 50, further including:

a chip package, wherein the monocrystalline semiconductor substrate is disposed in the chip package; and

a host, wherein the chip package is disposed in the host.

52. The electrical device according to claim 50, further including:

a chip package, wherein the monocrystalline semiconductor substrate is disposed in the chip package;

a host, wherein the chip package is disposed in the host, wherein the host includes a memory module; and

an electronic system, wherein the memory module is disposed in the electronic system.

53. The electrical device according to claim 50, further including:

a chip package, wherein the monocrystalline semiconductor substrate is disposed in the chip package;

a host, wherein the chip package is disposed in the host, wherein the host

includes a dynamic random access memory module; and

an electronic system, wherein the dynamic random access memory module is disposed in the electronic system.

54. The electrical device according to claim 50, further including:

a chip package, wherein the monocrystalline semiconductor substrate is disposed in the chip package;

a host, wherein the chip package is disposed in the host; and

an electronic system, wherein the host is disposed in the electronic system.

55. The electrical device according to claim 50, further including:

a second STI disposed in the monocrystalline semiconductor substrate in a direction parallel to the first STI.

56. An electrical device comprising:

a semiconductor substrate including an upper surface;

a recess disposed in the upper surface wherein the recess is covered with a substantially curvilinear bottom profile including epitaxial semiconductive material;

a first gate dielectric layer disposed over the epitaxial semiconductive material;

a floating gate film disposed over the first gate dielectric layer;

a second gate dielectric layer disposed over the floating gate film; and

an electrode disposed over the second gate dielectric layer.

57. The electrical device according to claim 56, further including:

a first shallow trench isolation (STI) structure disposed immediately adjacent the recess.

58. The electrical device according to claim 56, further including:

a first shallow trench isolation (STI) structure disposed immediately adjacent the recess; and

a second STI structure disposed in the semiconductor substrate in a direction parallel to the first STI.

59. The electrical device according to claim 56, further including:

a chip package, wherein the semiconductor substrate is disposed in the chip package; and

a host, wherein the chip package is disposed in the host.

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60. The electrical device according to claim 56, further including:

a chip package, wherein the monocrystalline semiconductor substrate is disposed in the chip package;

a host, wherein the chip package is disposed in the host, wherein the host comprises a chip set; and

an electronic system, wherein the chip set is disposed in the electronic system.

61. A computer system, comprising:

a processor;

a memory system coupled to the processor;

an input/output (I/O) circuit coupled to the processor and the memory system; and

a vertical transistor disposed in the processor, the vertical transistor including:

a semiconductor substrate comprising an upper surface;

a recess disposed in the upper surface, wherein the recess contains an epitaxial semiconductor film comprising more than three monolithic surfaces;

a gate dielectric layer disposed over the epitaxial semiconductor film; and

an electrode disposed in the recess over the gate dielectric layer.

62. The computer system according to claim 61, wherein the processor is disposed in a host selected from a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, and an aircraft.